

CLAIMS

What is claimed is:

Sub A17

- 1 1. A method for reducing pilot tone phase interference at the transmitter in a
2 discrete multi-tone (DMT) communications system comprising:
3 generating DMT signal segments REVERB and SEGUE with a pseudo-
4 random pattern generator using an initial pattern that minimizes the pilot tone phase
5 offsets in both segments; and
6 transmitting the above-defined REVERB and SEGUE signals in the DMT
7 initialization sequence.
- 1 2. The method of claim 1, further comprising:
2 generating ADSL-over-POTS DMT signal segments C-REVERB and C-
3 SEGUE with a pseudo-random pattern generator polynomial as defined by the ADSL
4 standard but using an initial pattern of 90 (0x05A); and
5 transmitting the C-REVERB and C-SEGUE signal in the DMT ADSL
6 standard initialization sequence.

1 3. A method for timing recovery at the receiver in a discrete multi-tone
2 (DMT) communications system comprising:
3 receiving a plurality of signals generated and transmitted by an associated
4 far-end transmission unit;
5 converting the plurality of received signals through an analog to digital
6 converter (ADC);
7 detecting a phase error on the received pilot tone;
8 applying the phase error to a phase locked-loop to generate a frequency
9 correction signal; and
10 using the frequency correction signal to modify the sampling time of the
11 ADC.

1 4. The method of claim 3, wherein the detection of phase error is
2 compensated by an offset based on the received signal segment in the initialization
3 sequence.

1 5. The method of claim 3, wherein the step of detecting a phase error is
2 performed with a state machine in communication with the ADC output and the input to
3 the phase locked-loop.

1 6. The method of claim 3, further comprising:
2 synchronizing a digital to analog converter (DAC) in the transmitting path
3 by using a sampling clock derived from the phase locked-loop controlled ADC.

1 7. A method for timing recovery at the receiver in a discrete multi-tone
2 (DMT) communications system comprising:
3 receiving a pilot tone generated and transmitted by an associated far-end
4 transmission unit along with other signal streams at a particular receiver;
5 converting the plurality of received signals through an analog to digital
6 converter (ADC) to create a digital signal stream;
7 detecting the cyclic prefix in the received digital signal stream;
8 zeroing out the received digital signal stream from the input to a phase
9 locked-loop while the cyclic prefix is present in the received signal stream to create a
10 frequency correction signal; and
11 using the frequency correction signal to modify the ADC sampling timing.

1 8. The method of claim 7, further comprising:
2 synchronizing a digital to analog converter (DAC) in the transmitting path
3 by using a sampling clock derived from the phase locked-loop controlled ADC.

1 9. A method for timing recovery at the receiver in a discrete multi-tone
2 (DMT) communications system comprising:
3 receiving a standard pilot tone generated and transmitted by an associated
4 far-end transmission unit along with other signal streams at a particular receiver;
5 converting the plurality of received signals through an analog to digital
6 converter (ADC) to create a digital signal stream;
7 detecting the cyclic prefix in the received signal stream;
8 performing a time-domain equalization on the received signal stream;
9 removing the cyclic prefix portion of the equalized digital signal stream
10 from the input to a phase locked-loop to create a frequency correction signal; and
11 using the frequency correction signal to modify the sampling time of the
12 ADC.

1 10. The method of claim 9, further comprising:
2 synchronizing a digital to analog converter (DAC) in the transmitting path
3 by using a sampling clock derived from the phase locked-loop controlled ADC.

1 11. A method for timing recovery at the receiver in a discrete multi-tone
2 (DMT) communications system comprising:
3 receiving a standard pilot tone generated and transmitted by an associated
4 far-end transmission unit along with other signal streams at a particular receiver;
5 converting the plurality of received signals through an analog to digital
6 converter (ADC) to create a digital signal stream;
7 detecting the cyclic prefix in the received signal stream;
8 using the equalized signal stream with the cyclic prefix portion removed to
9 estimate the phase error with a discrete Fourier transform (DFT);
10 applying the estimated phase error to the input of a phase locked-loop to
11 create a frequency correction signal; and
12 using the frequency correction signal to modify the sampling time of the
13 ADC.

1 12. The method of claim 11, further comprising:
2 synchronizing a digital to analog converter (DAC) in the transmitting path
3 by using a sampling clock derived from the phase locked-loop controlled ADC.

1 13. A digital signal processor configured to apply the method of claim 1.

1 14. A digital signal processor configured to compensate for the offset in phase
2 error on a received pilot tone based upon the received signal segment in the discrete
3 multi-tone (DMT) system initialization sequence.

1 15. The digital signal processor of claim 14, wherein the phase error
2 compensation is accomplished with a state machine.

1 16. A digital signal processor configured to detect and zero out the cyclic
2 prefix from a received digital signal stream when the cyclic prefix is present to create an
3 input to a phase locked-loop.

1 17. The digital signal processor of claim 16, wherein the digital signal
2 processor is configured to perform a time-domain equalization on a received digital data
3 stream and to create an input to a phase locked-loop when the cyclic prefix is zeroed out
4 from the signal stream.

1 18. A digital signal processor configured to detect and remove the cyclic
2 prefix from a received digital signal stream when the cyclic prefix is present, the digital
3 signal processor further configured to first perform a time-domain equalization of the
4 digital signal stream, then to perform a discrete Fourier transform on the digital signal
5 stream when the cyclic prefix is not present to create a phase error signal for application
6 at the input to a phase locked-loop.

1 19. A system for timing recovery in a discrete multi-tone communications
2 system comprising:
3 an analog to digital converter (ADC);
4 a state machine in communication with the ADC configured to determine
5 the phase offset on a pilot tone in a received signal segment; and
6 a phase locked-loop in communication with the state machine configured
7 to compensate for the phase offset and to apply a control signal to the ADC, wherein the
8 received signal samples are synchronized for further processing at a rate compatible with
9 that of a source transmission.

1 20. The system of claim 19, further comprising:
2 a sampling clock in communication with the analog to digital converter,
3 the sampling clock in further communication with a digital to analog converter (DAC) in
4 an upstream data path for synchronizing data transmitted in an upstream direction to the
5 source.

1 21. A system for timing recovery in a discrete multi-tone communications
2 system comprising:
3 an analog to digital converter (ADC) configured to create a digital
4 representation of the received signal;
5 a phase locked-loop in communication with the ADC configured to
6 receive the received signal and to apply a control signal to the ADC, wherein the received
7 signal sample stream is synchronized for further processing at a rate compatible with that
8 of a source transmission; and
9 a symbol synchronizer in communication with the ADC configured to
10 determine when the data stream contains a cyclic prefix, the symbol synchronizer further
11 configured to remove the received signal from the phase locked-loop input when the
12 cyclic prefix is present.

1 22. The system of claim 21, further comprising:
2 a sampling clock in communication with the analog to digital converter,
3 the sampling clock in further communication with a digital to analog converter (DAC) in
4 the transmitting path for synchronizing data transmitted in the reverse direction to the far-
5 end transmission unit.

1 23. A system for timing recovery in a discrete multi-tone communications
2 system comprising:
3 an analog to digital converter (ADC) configured to create a digital
4 representation of the received signal;
5 an equalizer in communication with the ADC, the equalizer configured to
6 perform a time-domain equalization on the received signal;
7 a phase locked-loop in communication with the ADC and the equalizer
8 configured to receive the received signal and to apply a control signal to the ADC,
9 wherein the received signal sample stream is synchronized for further processing at a rate
10 compatible with that of a source transmission; and
11 a symbol synchronizer in communication with the ADC configured to
12 determine when the signal stream contains a cyclic prefix, the symbol synchronizer
13 further configured to remove the time-domain equalized signal from the phase locked-
14 loop input when the cyclic prefix is present.

1 24. The system of claim 23, further comprising:
2 a sampling clock in communication with the analog to digital converter ,
3 the sampling clock in further communication with a digital to analog converter (DAC) in
4 the transmitting path for synchronizing signal transmitted in the reverse direction to the
5 far-end transmission unit.

1 25. A system for timing recovery in a discrete multi-tone communications
2 system comprising:
3 an analog to digital converter (ADC) configured to create a digital
4 representation of the received signal;
5 an equalizer in communication with the ADC, the equalizer configured to
6 perform a time-domain equalization on the received signal;
7 a discrete Fourier transform (DFT) in communication with the equalizer,
8 the DFT configured to convert the time-equalized received signal and to generate a pilot
9 tone phase error estimate signal;
10 a symbol synchronizer in communication with the ADC configured to
11 remove the cyclic prefix from the signal sample stream; and
12 a phase locked-loop in communication with the ADC and the DFT configured to
13 receive the pilot tone phase error estimate and to apply a control signal to the ADC,
14 wherein the received signal sample stream is synchronized for further processing at a rate
15 compatible with that of a source transmission.

1 26. The system of claim 25, further comprising:

2 a sampling clock in communication with the analog to digital converter ,
3 the sampling clock in further communication with a digital to analog converter (DAC) in
4 the transmitting path for synchronizing signal transmitted in the reverse direction to the
5 far-end transmission unit.

1 27. A system for timing recovery at the receiver in a discrete multi-tone
2 (DMT) communications system comprising:

3 means for receiving a pilot tone generated and transmitted by an associated
4 far-end transmission unit;

5 means for converting the received pilot tone along with the other received
6 signals from an analog to a digital signal;

7 means for detecting a phase error on the received pilot tone;

8 means for applying the phase error to a phase locked-loop to generate an
9 output signal responsive to when the cyclic prefix is not present in the digital signal; and

10 means for using the output signal to modify the analog to digital
11 conversion timing.

- 1 28. A method for timing recovery at the receiver in a discrete multi-tone
2 (DMT) communications system comprising:
3 means for receiving a standard pilot tone and far-end signal from an
4 associated far-end transmission;
5 means for converting the plurality of received signals from analog to
6 digital signals;
7 means for detecting the cyclic prefix in the received far-end signal;
8 means for removing the cyclic prefix in the received far-end signal;
9 means for estimating the phase error in the pilot tone with a discrete
10 Fourier transform (DFT);
11 means for applying the estimated phase error to the input of a phase
12 locked-loop to create a frequency correction signal; and
13 means for using the frequency correction signal to modify the sampling
14 rate of the analog to digital conversion.

1 29. A method for timing recovery at the receiver in a discrete multi-tone
2 (DMT) communications system comprising:
3 means for receiving a standard pilot tone along with a plurality of signals
4 at this particular receiver from a far-end signal;
5 means for converting the plurality of signals from analog to digital signals;
6 means for performing a time-domain equalization on the far-end signal;
7 means for detecting the cyclic prefix in the far-end signal;
8 means for zeroing out the equalized digital signal from the input to a phase
9 locked-loop while the cyclic prefix is present in the received signal to create frequency
10 correction signal; and
11 means for using the frequency correction signal to modify the sampling
12 rate of the analog to digital conversion.

1 30. A method for timing recovery at the receiver in a discrete multi-tone
2 (DMT) communications system comprising:
3 means for receiving a far-end signal along with a plurality of signals at the
4 receiver;
5 means for converting the plurality of received signals from an analog to a
6 digital format;
7 means for detecting the cyclic prefix in the far-end signal;
8 means for zeroing out the far-end signal when the cyclic prefix is present
9 from the input to a phase locked-loop; and
10 means for using the phase locked-loop output to modify the sampling rate
11 of the analog to digital conversion.

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